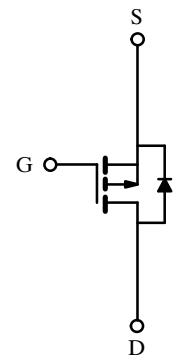
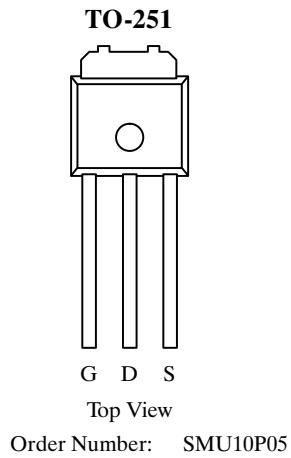
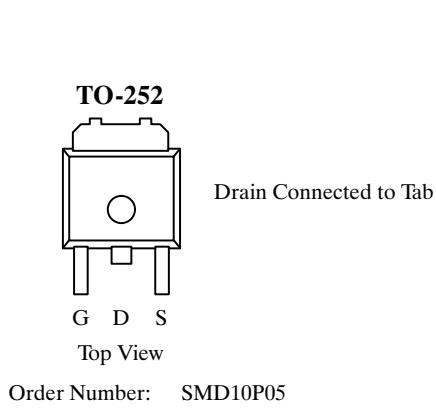


P-Channel Enhancement-Mode Transistors

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D^a (A)
-50	0.28	-10

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-50	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^b	I_D	-2.0	A
		-1.3	
Pulsed Drain Current (maximum current limited by package)	I_{DM}	-16	
Power Dissipation	P_D	40	W
		2.0 ^b	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 sec.)	T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient Free Air, PC Board Mount ^b	R_{thJA}	50	60	°C/W
Junction-to-Ambient Free Air, Vertical Mount		50	60	
Junction-to-Case		2.3	3.0	

Notes:

- a. Calculated Rating for $T_C = 25^\circ\text{C}$, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
- b. Surface mounted on PC board or mounted vertically in free air.

Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

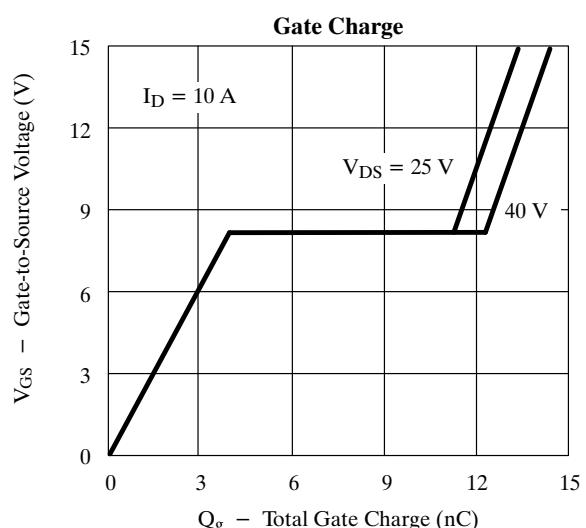
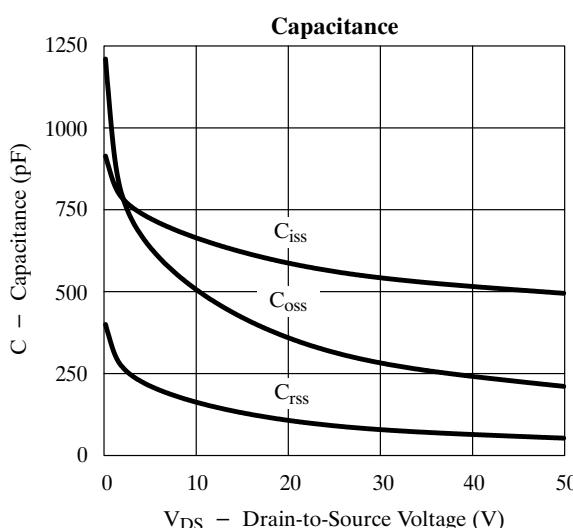
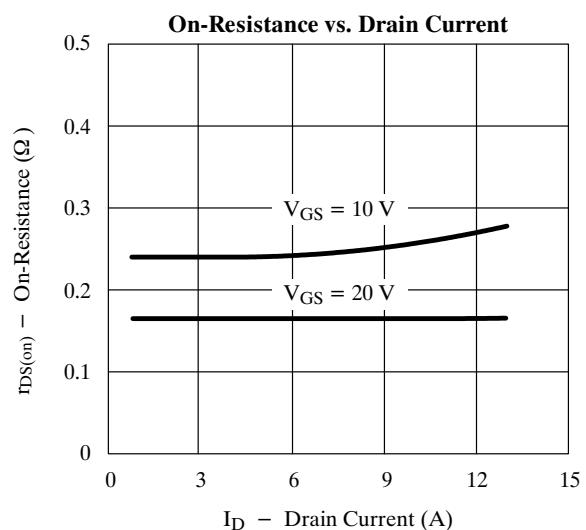
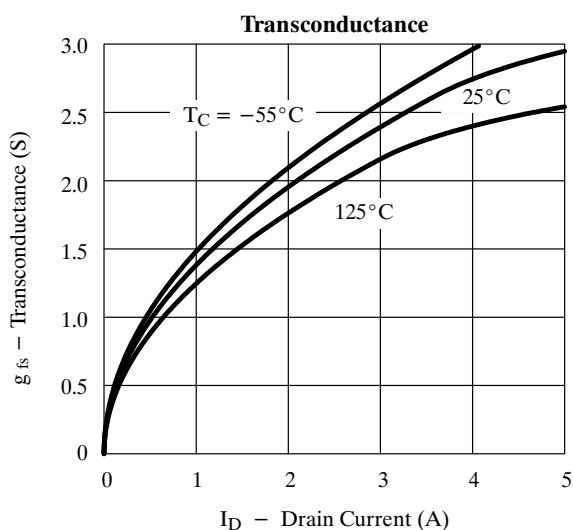
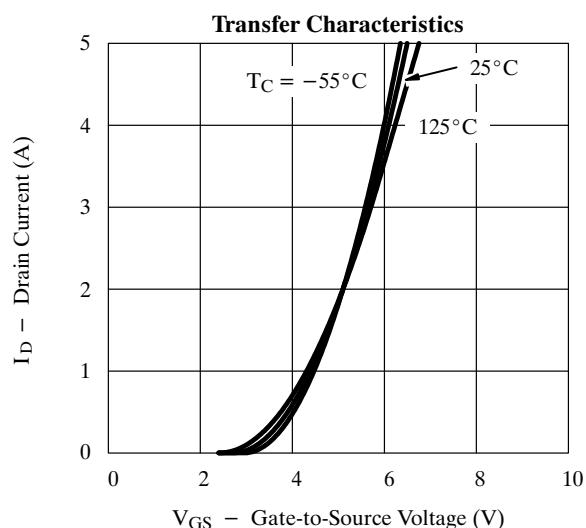
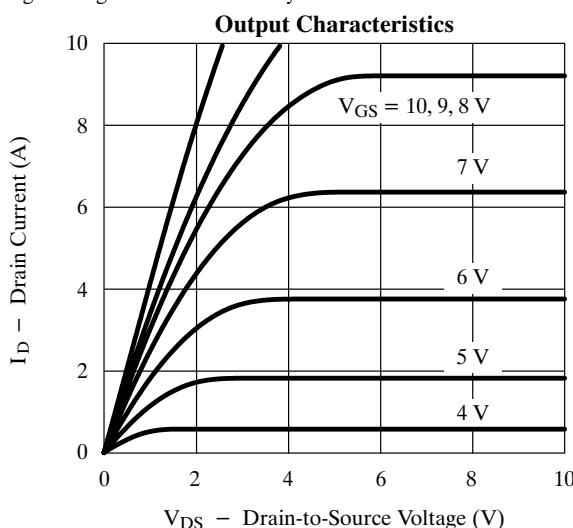
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-50			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-2.0		-4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}$			-25	
		$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$			-250	μA
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-10			A
Drain-Source On-State Resistance ^b	$r_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$		0.25	0.28	
		$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}, T_J = 125^\circ\text{C}$		0.4	0.50	Ω
Forward Transconductance ^b	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -5 \text{ A}$	1.0	3		S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$		530		pF
Output Capacitance	C_{oss}			325		
Reverse Transfer Capacitance	C_{rss}			85		
Total Gate Charge ^c	Q_g	$V_{DS} = -25 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$		13	20	nC
Gate-Source Charge ^c	Q_{gs}			3.6	5.0	
Gate-Drain Charge ^c	Q_{gd}			9	12.0	
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = -30 \text{ V}, R_L = 3 \Omega$ $I_D = -10 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 25 \Omega$		10	30	ns
Rise Time ^c	t_r			50	95	
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			25	90	
Fall Time ^c	t_f			50	75	
Source-Drain Diode Ratings and Characteristics						
Continuous Current	I_S				-2.0	A
Pulsed Current	I_{SM}				-24	
Forward Voltage ^b	V_{SD}	$I_F = -2 \text{ A}, V_{GS} = 0 \text{ V}$			-2.3	V
Reverse Recovery Time	t_{rr}	$I_F = -2 \text{ A}, dI_F/dt = 100 \text{ A}/\mu\text{s}$		70		ns
Reverse Recovery Charge	Q_{rr}			0.07		μC

Notes:

- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width duty cycle 1%.
- c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

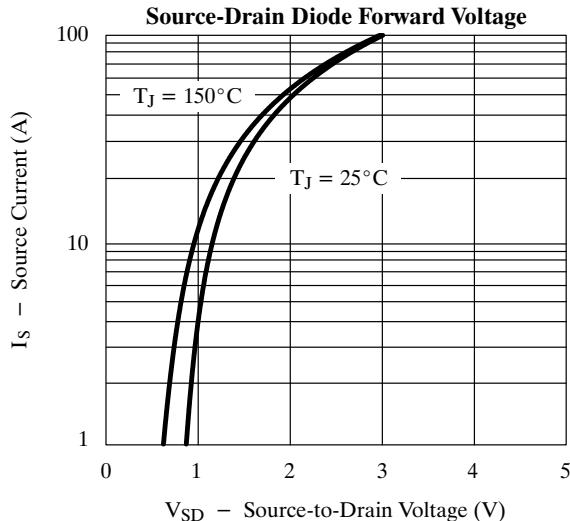
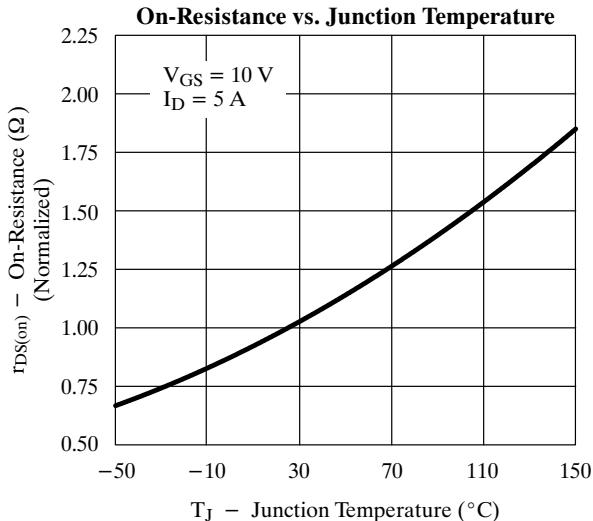
Negative signs omitted for clarity.



SMD/SMU10P05

Typical Characteristics (25°C Unless Otherwise Noted)

Negative signs omitted for clarity.



Thermal Ratings

